bus inputs and a[n] plurality of bus outputs, with the central unit [being capable of] selectively coupling at least one of the inputs to [the] at least one of the outputs, the central unit [adapted to provide] providing for an arbitrated, point-to-point coupling of a particular one of the plurality of bus elements with the at least one other bus element;

(c) a first plurality of uni-directional point-to-point buses for coupling in a first predetermined direction the bus elements to the central unit bus inputs;

(d) a second plurality of uni-directional point-to-point buses for coupling in a second predetermined direction [the] each output of the central unit to [each of the] a respective bus element[s]; and

(e) arbitration logic connected to the plurality of bus inputs of the central unit to which the first plurality of uni-directional point-to-point buses connect, the arbitration logic [being capable of] for granting each of the bus elements access to the at least one other bus element through the central unit one at a time based upon the requests from the bus elements.

30. (Thrice Amended) A system comprising:

a plurality of central processing units;

a shared memory;

a central unit including:

combining logic including a respective cpu input for each of the plurality of central processing

units, a respective cpu output for each of the plurality of central processing units, a shared memory input, and a shared memory output, the combining logic for selectively coupling at least one of the cpu inputs to the shared memory output and for selectively coupling the shared memory input to at least one of the cpu outputs;

[combining logic for accepting a plurality of parallel inputs, the plurality of parallel inputs at least equal to the number of the central processing units plus memory and coupling at least one of its inputs to its output;]

arbitration logic coupled to the combining logic for controlling which of the cpu inputs is provided at the shared memory output and for controlling which of the cpu outputs is coupled to the shared memory input;

a memory controller providing [a] the shared memory input to the combining logic and receiving [a] the shared memory output from the combining logic;

a plurality of first uni-directional point-to-point buses, with one bus coupling each of the central processing units to an input of the combining logic, and with each of the first uni-directional point-to-point buses for coupling in a first predetermined direction a central processing unit to an input of the combining logic;

a first uni-directional memory bus for coupling in a second predetermined direction the memory to the memory controller;

a plurality of second uni-directional point-

to-point buses for coupling in a third predetermined direction the output of the combining logic to the central processing units; and

a second uni-directional memory bus for coupling in a fourth predetermined direction the output of the memory to the memory control logic.

33. (Thrice Amended) A method of implementing a high speed bus to which a plurality of bus elements are coupled comprising the steps of:

(a) coupling, with a first uni-directional bus in a first predetermined direction, each of the bus elements to a central unit via one of a plurality of first bus inputs;

(b) selecting with arbitration means one of the first bus inputs to the central unit [to be an] for output to one of a plurality of central unit outputs;

(c) coupling with a second uni-directional bus in a second predetermined direction, each of the plurality of central unit outputs to a respective one of the plurality of [said output to each of the] bus elements; and

(d) providing for an arbitrated, point-to-point coupling of a particular one of the plurality of bus elements with at least another bus element.